

Appl. No. 10/777,990

Response dated: August 4, 2005

Reply to Office action of May 4, 2005

• **Amendments to the Claims:**

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1. (Currently Amended) A mother substrate comprising:
a plurality of display cells, each of the display cells having an inspection line receiving a first inspection signal externally provided, a driving part outputting a second inspection signal in response to the first inspection signal provided through the inspection line, and a pixel part being driven in response to the second inspection signal; and
an inspecting pad part extended from the inspection line so as to provide the first inspection signal to the inspection line,
wherein the inspection line comprises:
a plurality of input lines connected to the driving part and spaced apart from each other in a predetermined distance; and
a connecting line electrically connected between the input lines, and electrically connected between the input lines and the inspecting pad part.
2. (Original) The mother substrate of claim 1, wherein the pixel part comprises a plurality of pixels, each of the pixels having a gate line, a data line substantially perpendicular to the gate line and a switching device connected to the gate and data lines.
3. (Original) The mother substrate of claim 2, wherein the driving part comprises a shift register having a plurality of stages so as to output the second inspection signal to the gate line.
4. (Original) The mother substrate of claim 3, wherein the first inspection signal has a voltage level suitable for substantially simultaneously driving the stages.
5. (Canceled)

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6. (Currently Amended) The mother substrate of claim 5, wherein the input lines comprise a start signal input line, a clock input line and a driving voltage input line so as to receive signals used to drive the driving part.

7. (Original) The mother substrate of claim 6, wherein the start signal input line is connected to a first stage of the stages.

8. (Original) The mother substrate of claim 6, wherein the clock input line comprises a first clock input line that receives a first clock and a second clock input line that receives a second clock.

9. (Original) The mother substrate of claim 6, wherein the driving voltage input line receives a ground voltage.

10. (Currently Amended) A substrate for a display panel, comprising:
a lower substrate having an inspection line receiving a first inspection signal externally provided, a driving part outputting a second inspection signal in response to the first inspection signal provided through the inspection line, and a pixel part being driven in response to the second inspection signal; and
an upper substrate being coupled to the lower substrate,
wherein the driving part has a plurality of first switching devices formed on the lower substrate, and the pixel part has a plurality of second switching devices formed on the lower substrate.

11. (Original) The substrate of claim 10, wherein the inspection line comprises:
a plurality of input lines spaced apart from each other in a predetermined distance; and
a connecting line electrically connected between the input lines.

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12. (Currently Amended) The substrate of claim 11, wherein an end portions of the input lines are disposed on an edge portion of the lower substrate, and a connecting line electrically connected between the end portions of the input lines is disposed on the edge portion of the lower substrate.

13. (Currently Amended) The substrate of claim 12, wherein the lower substrate is partially grinded, the end portions of the input lines disposed on the edge portion and a portion of the connecting line disposed on the edge portion are removed while the lower substrate is grinded.

14. (Currently Amended) The substrate of claim 13, wherein the input lines comprises a start signal input line, a clock input line and a driving voltage input line.

15. (Original) The substrate of claim 14, wherein the driving voltage input line has a width wider than those of the start signal input line and clock input line.

16. (Original) The substrate of claim 15, wherein the driving voltage input line receives a first inspection signal externally provided, and provides the first inspection signal to the inspection line.

17. (Original) The substrate of claim 10, further comprising a liquid crystal layer disposed between the lower substrate and the upper substrate.

18. (Currently Amended) A method of manufacturing a display panel, comprising:
fabricating a substrate for a display panel, the substrate having a lower substrate and an upper substrate coupled to the lower substrate, the lower substrate having an inspection line receiving a first inspection signal externally provided, a driving part outputting a second inspection signal in response to the first inspection signal provided through the inspection line, and a pixel part being driven in response to the second inspection signal;

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providing the first inspection signal to the inspection line to inspect the driving part and pixel part; and

insulating the inspection line from the an input line to complete the display panel, wherein the driving part and the pixel part are formed on the lower substrate.

19. (Original) The method of claim 18, further comprising:

fabricating a mother substrate for the lower substrate having an inspecting pad part extended from the inspection line;

providing the first inspection signal to the inspecting pad part to inspect the mother substrate for the lower substrate;

fabricating a mother substrate for the upper substrate;

combining the mother substrate for the lower substrate with the mother substrate for the upper substrate; and

cutting the combined substrate to complete the substrate for the display panel.

20. (Original) The method of claim 18, wherein the inspection line is removed by grinding an edge of the substrate for the display panel.

21. (New) The mother substrate of claim 1, wherein the driving part has a plurality of first switching devices formed on the lower substrate via a thin film process, and the pixel part has a plurality of second switching devices formed on the lower substrate via the thin film process.

22. (New) The substrate of claim 14, wherein the clock input line comprises a first clock input line that receives a first clock and a second clock input line that receives a second clock.

23. (New) The method of claim 18, wherein the driving part has a plurality of first amorphous silicon transistors formed on the lower substrate, and the pixel part has a plurality of second amorphous silicon transistors.